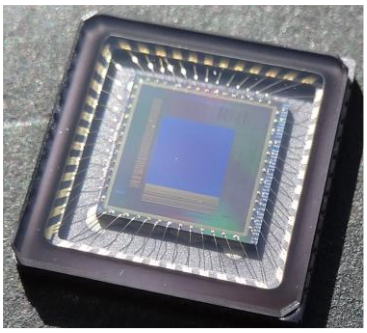
UIC1203R - optical sensor IC for detection and processing of the dynamic targets

Description



The UIC1203R is CMOS image sensor for detection and identification of quickly changing (moving and changing brightness) small-sized targets (light spots) at the conditions of strongly non-uniform and slowly changing in time background.

Sensor internally defines the image characteristics that are detected from synchronous, asynchronous and constant light sources.

The image processing algorithm provides the definition of X and Y coordinates, the areas and brightness levels of 8 targets simultaneously.

Fixed Pattern Noise (FPN) is effectively suppressed by a special algorithm using accumulation and subtraction of background frame. Background frame can be done as adaptive to scene.

Usage of column parallel 10-bit ADC allows to reach the frame frequency till 2.5K fps.

Sensor control (configuration) and reading of targets characteristics are realized through the SPI-interface. Video image can be read via parallel 10-bit data-bus.

Sensor can be built in multi-element systems due to broadcast mode.

UIC1203R is intended for technical vision systems, demanding high sensitivity, high frame frequency and internal definition of image parameters.

Application

- tracking systems of quickly moving objects
- sensors of move detection
- contactless measurement of small movements (optical joystick, metric gauges)
- rotation angle gauges
- devices for position stabilization
- coordinate gauges for games (simulator and shooter types)
- training simulators
- optical navigation systems
- helmet of the virtual reality

Key Specifications

Feature		Value	Units
Array size		128 x 128	pixels
Pixel size		20.16 x 20.16	μm^2
Image field size		2.58 x 2.58	mm^2
Lens size		1/5"	
Fill factor		90	%
Spectral range		0.36 - 1.05	µm
Quantum efficiency		> 60	%
Noise equivalent exposition, λ = 0.7 µm		$5.6 \cdot 10^{-12}$	J/cm^2
Integral noise equivalent exposition, source A-type		$2.4 \cdot 10^{-6}$	lux· second
Clock frequency, F_{CLK}		till 100	MHz
Frame rate, Fclk=50 MHz		~ 1300	fps
Row time, T_{ROW}		292	T_{CLK}
Full exposure interval	min	129	T_{ROW}
	max	128+65536	
Exposure interval (F_{CLK}=50 MHz, T_{CLK}=20 ns)	min	~ 0,75	sec^{-3}
	max	~ 38	
Exposure type		Rolling Shutter	
Quantity of targets per frame		8	
Defined characteristics of targets		X-,Y-coordinates, S- square, A - brightness	
Accuracy of coordinates determination		0.01	pix
		0.2	µm
Interface type		SPI	
Clock frequency SPI, F_{SCLK}		< F_{CLK} /4	
Parallel digital video output		10 bit	
Synchronization		DSYN — data HSYN — row VSYN — frame	
Power supply, core / IO		1.8 / 3.3	V
Power consumption		< 60	mW
Package type		PLCC-48	
		COB	

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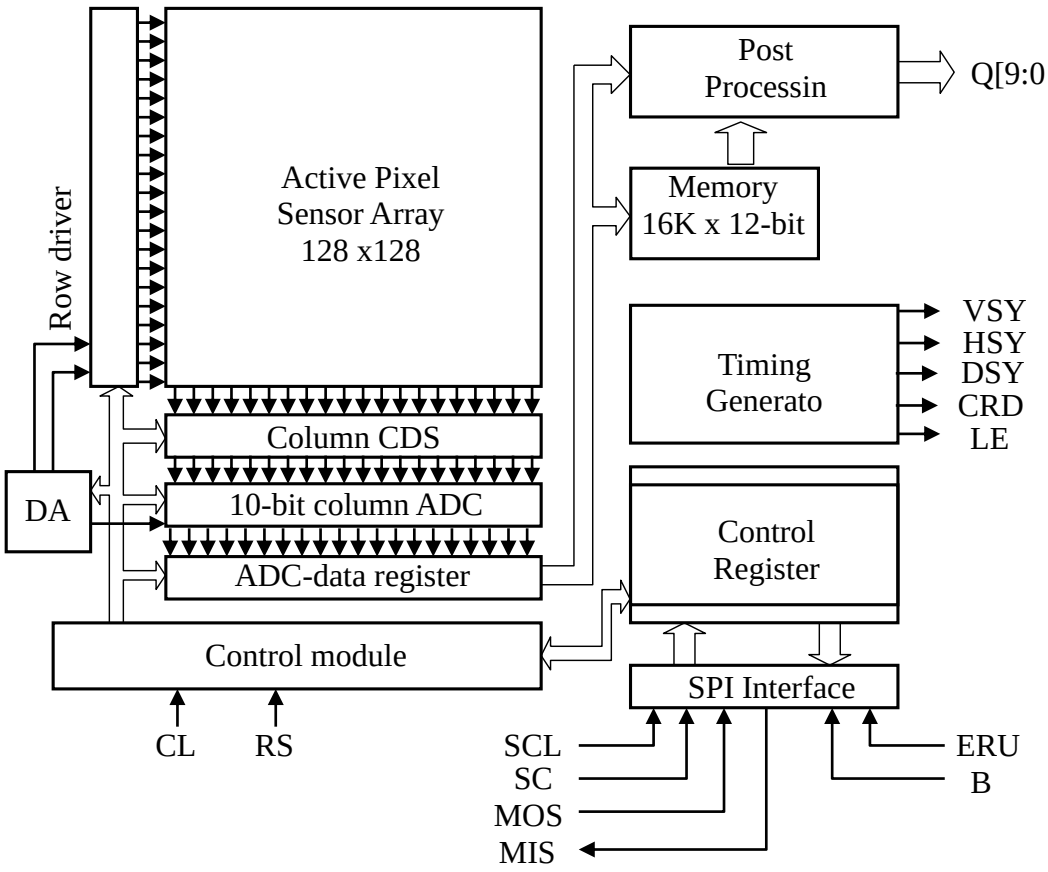
UIC1203R Block Diagram



Active Pixel Array has 128x128 high sensitive and fast pixels with 20.16 µm pixel pitch. Fill Factor is more than 90%, spectral range is (0.36 — 1.05) µm.

Row Driver forms the control signals (RST, TX, SR) for row of pixels.

Column CDS – Correlated Double Sampling for noise elimination.

10-bit column ADC – scheme for analog-to-digital conversion of video signal. Each column has a comparator circuit. The video signal after CDS circuit gets to comparator input. Other comparator input is used for searching of digital equivalent of video signal by bisection algorithm.

ADC-data register – parallel/series digital register for 10-bit video signal after ADC.

Control module with **Control Registers** – digital blocks for sensor modes tuning and configuration. These blocks are intended for forming of timing diagram and for management of internal interaction.

DAC block consists of some internal DACs intended for forming of non-standard reference

voltages.

Memory block is used for storage of background frame's data. These data can be written directly or by adaptive algorithm. The data of storage frame can be subtracted from data of current frame with getting of difference frame data.

Post Processing module works with difference frame data and performs the following functions:

- detection of pixels with signal more than defined threshold
- analysis of the selected pixels by connectivity, formation of targets in pixel's area
- calculation of X and Y coordinates for positions of target's gravity centers with 0.01 pix accuracy
- calculation of the areas and integral brightness for 8 targets
- defining of target form proportion (picture compression)
- recording the following data to output SPI registers:
  - index of target existence in a frame
  - target's quantity and parameters
  - data of current pixel of background frame
- forming of Q[9:0] output data bus

Timing Generator forms the output signals of data (DSYN), row (HSYN) and frame (HSYN) synchronization. Also it forms the signal of coordinate data ready (CRDY) and external light source synchronizing pulse (LED).

SPI Interface is 4-wire bidirectional serial interface block. It is intended for data record to the control registers, and for data read from output SPI registers.
Additionally 2 control signal can be used:

- ERUN – external start signal for group of sensors
- BE – Broadcast Enable signal for transfer of MISO output to high impedance state.

Electrical characteristics

DC characteristics.
T_A= -20 to +60 °C, C_L = 15 pF

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Operating voltage	DVDD VDD VDA VDDA VDPIX VCC	Applied to DVDD pins Applied to VDD pins Applied to VDA pins Applied to VDDA pins Applied to VDPIX pins Applied to VCC pins	3.0 1.62 1.7 1.7 1.7 3.15	3.3 1.8 1.8 1.8 1.8 3.3	3.6 1.98 1.9 1.9 1.9 3.45	V
Total power consumption	P_{TOT}	F_{CLK} =50 MHz	-	60	65	mW
Input voltage	V_{IH}	-	2.0	-	5.5	V
	V_{IL}	-	-0.3	-	0.8	
Output voltage	V_{OH}	I_{OH} < 2mA	2.4	-	3.6	V
	V_{OL}	I_{OL} < 2mA	0	-	0.4	

Characteristics	Symbol	F_{CLK} , MHz			Unit	Conditions
		12	24	48		
Supply current	I_{DVDD} I_{VDD} I_{VDA} I_{VDDA} I_{VDPIX} I_{VCC}	0.2 1.2 5.5 0.02 4.2 0.45	0.3 2.4 5.5 0.03 4.2 0.45	0.5 4.6 5.5 0.05 4.2 0.45	mA	Default mode, EXP=1 0 lux illumination

AC characteristics.
DVDD=3.3V±0.3V, VDD=1.8V±0.18V, T_A= -20 to +60 °C, C_L = 10 pF

Characteristics	Symbol	Min	Typ	Max	Unit
Main input clock frequency	F_{CLK}	1	50	100	MHz
Data output clock frequency	F_{DATA}	0.5	25	50	
SPI clock frequency	F_{SPI}	F_{CLK}/4	12	25	

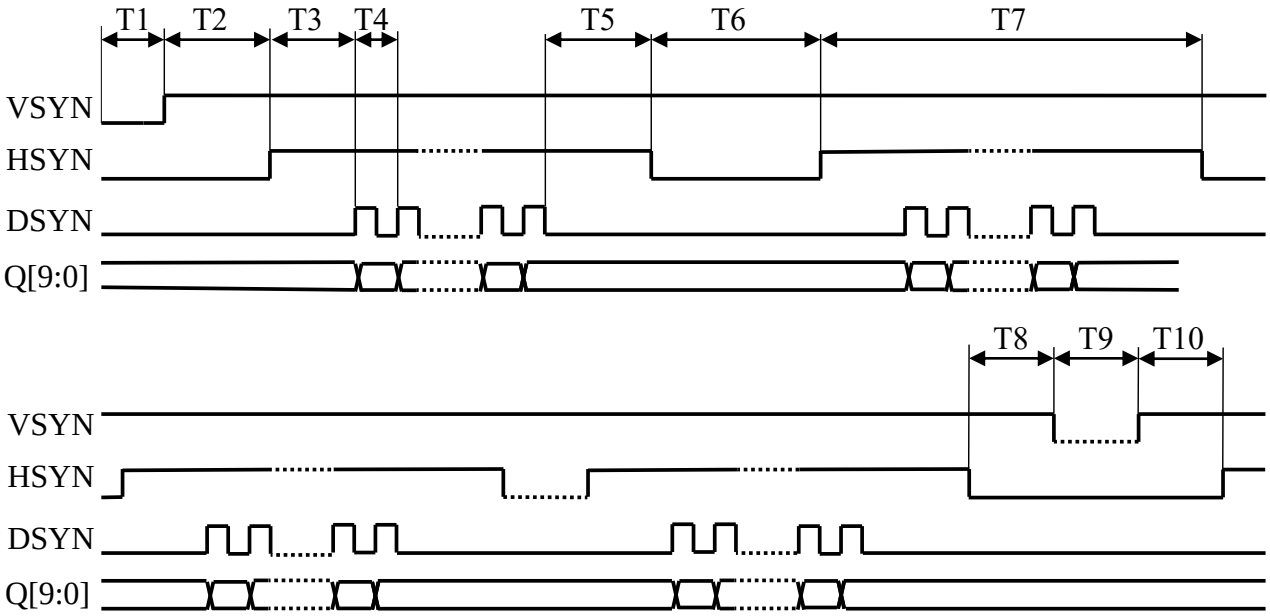
Control and Configuration Registers

Sub-address (hex)	Register	Default (hex)	Description
10	CONTROL	0	Start control RUN[2] – "1" sensor start, "0" – sensor stop
11	CONFIG	0410	Configuration register CONFIG[4] – GMODE – adaptive background mode CONFIG[5] – EKL – test mode CONFIG[6] – DMODE CONFIG[7] – AMODE CONFIG[8] – OU – output bus Q[9:0] enable CONFIG[9:10] – KRL[0:1] - target form proportion (picture compression) CONFIG[11] – MB – Memory Blocking CONFIG[12] – AV – Aperture (3x3 pix) enable CONFIG[13] – ASD – memory (read "0")/(write "1") at AMOD CONFIG[14] – PHS – polarity of HSYN CONFIG[15] – PVS– polarity of VSYN
12	EXP	1	EXP[15:0] – exposure control Exposure time T_{EXP} = (128 x T_{ROW}) + (T_{ROW} x EXP[15:0]) T_{ROW} = 292 x T_{CLK}
20	TC_RST		RST pulse position
21	TC_F1		F1 pulse position
22	TC_TX		TX pulse position
23	TC_F2		F2 pulse position
24	TC_CS		CS pulse position
25	TC_EKL		EKL pulse position
			Control of pixel reading and CDS signals
26	RTM	0	RTM signal enable
30	KODR	7	KODR[3:0] – control of internal DAC VRST
31	KODW	1E	KODW[7:0] – control of internal DAC VW
32	KODT	40	KODT[7:0] – control of internal DAC VTX
33	RUNB	F	RUNB[3:0] – control of internal BIAS modes
34	DRES	87	DRES[7:0] – control of ADC range
35	KODV	FA	KODV[7:0] – control of internal DAC VDR
40	POR	7F	POR[9:0] – control of threshold level for target definition
41	RAF	3	RAF[2:0] – control of adaptation speed for background frame

Basic principles of UIC1203R.

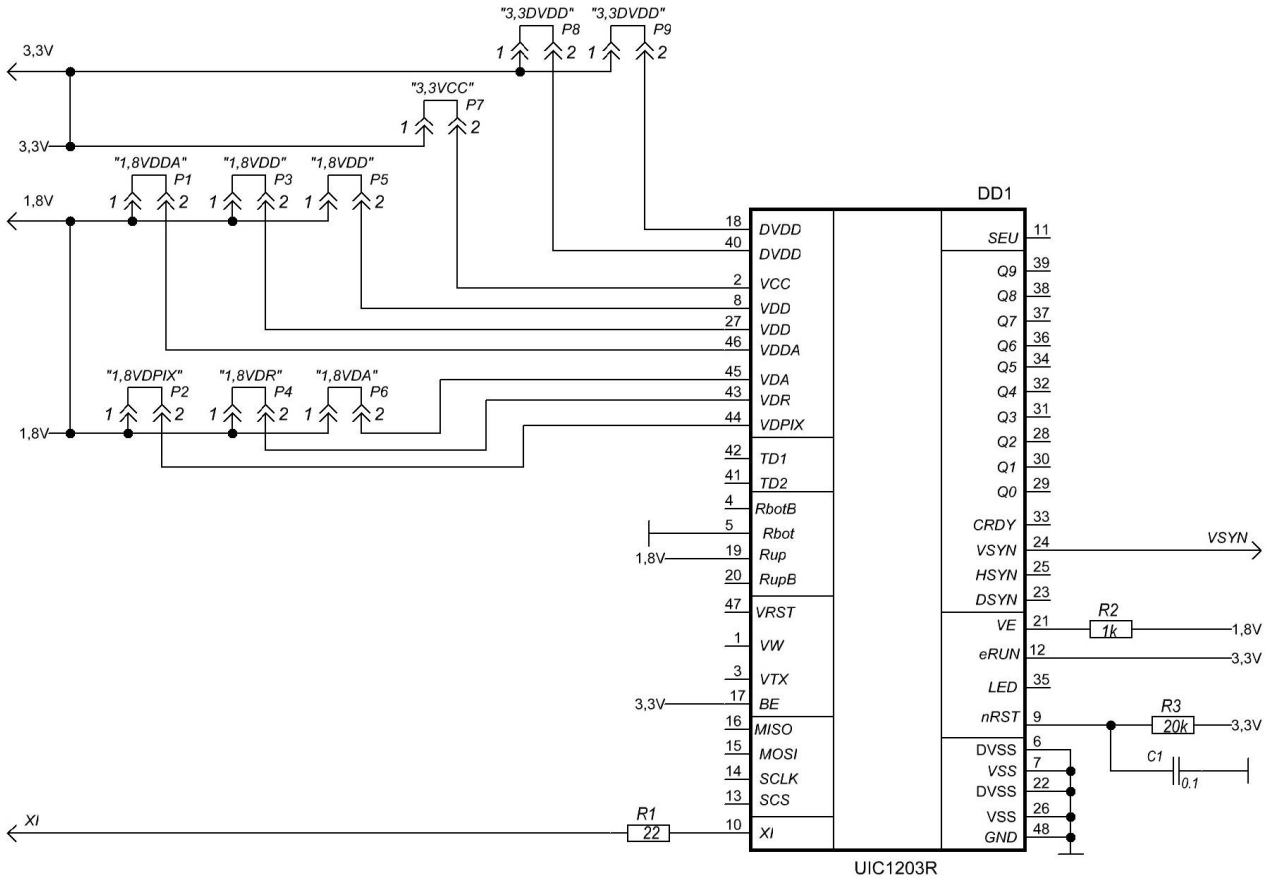
- UIC1203R is controlled by 4-wire SPI interface.
- Sensor timing diagram and internal reference voltages are formed by configuration of SPI registers in control block and DAC block.
- UIC1203R use Rolling Shutter type of frame scanning. Exposure time is controlled by SPI register.
- While frame scanning the analog video signal from pixels of the selected row is transferred to column amplifiers. Correlated Double Sampling circuit is used for noise elimination.
- After CDS the video signal transfers to a comparator input. Another comparator input is used for searching of digital equivalent of video signal by bisection algorithm. Resulting 10-bit digital video signal records to ADC-data column registers.
- Digital video signal is transmitted to Memory block with one frame capacity. The data recording method depends on the selected mode (DMOD, AMOD, GMOD).
- At DMOD and AMOD the direct background frame is written to a memory. The direct background frame is dark frame with minimum exposure time or with closed optical lens.
- At GMOD mode the average background frame is stored and changes according to the special procedure of the adaptive accumulation.
- The data of storage frame are subtracted from data of current frame with getting of clear difference frame data.
- Difference frame is transferred via threshold scheme, that passes only pixels with level above a threshold POR.
- The processing block uses this data for target selecting and calculation of target's characteristics.
- Target's characteristics are recorded to output SPI register.

Timing diagram for synchronizing pulses VSYN, HSYN, DSYN and output data Q[9:0].

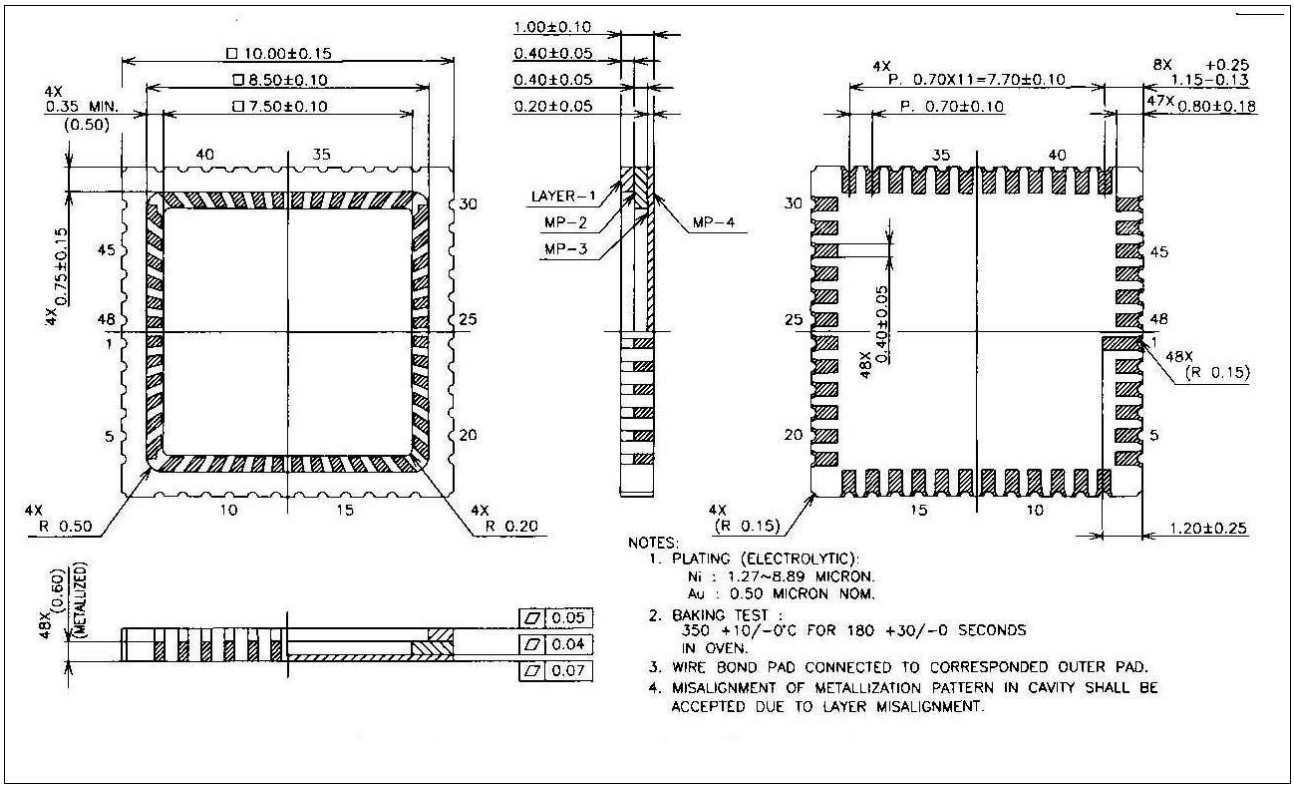


T1. Initial state.
T2. Frame start. Delay between VSYN and HSYN. Duration of T2 = 291 x T_{CLK}.
T3. Start of data output. Duration of T3 = 2 x T_{CLK}.
T4. 1st image pixel time. Duration of DSYN T_{DSYN} = 2 x T_{CLK}.
T5. End of Row time. Duration of T5 = 3 x T_{CLK}.
T6. Interline time interval. Duration of T6 = 32 x T_{CLK}.
T7. Duration of Row synchronizing T7 = 260 x T_{CLK}.
T8. End of Frame time. Duration of T8 = 32 x T_{CLK}.
T9. Interframe time interval. Duration of T9 = 292 x T_{CLK} x EXP +1.
T10. Next frame start. Delay between VSYN and HSYN. Duration of T10 = T2 = 291 x T_{CLK} .

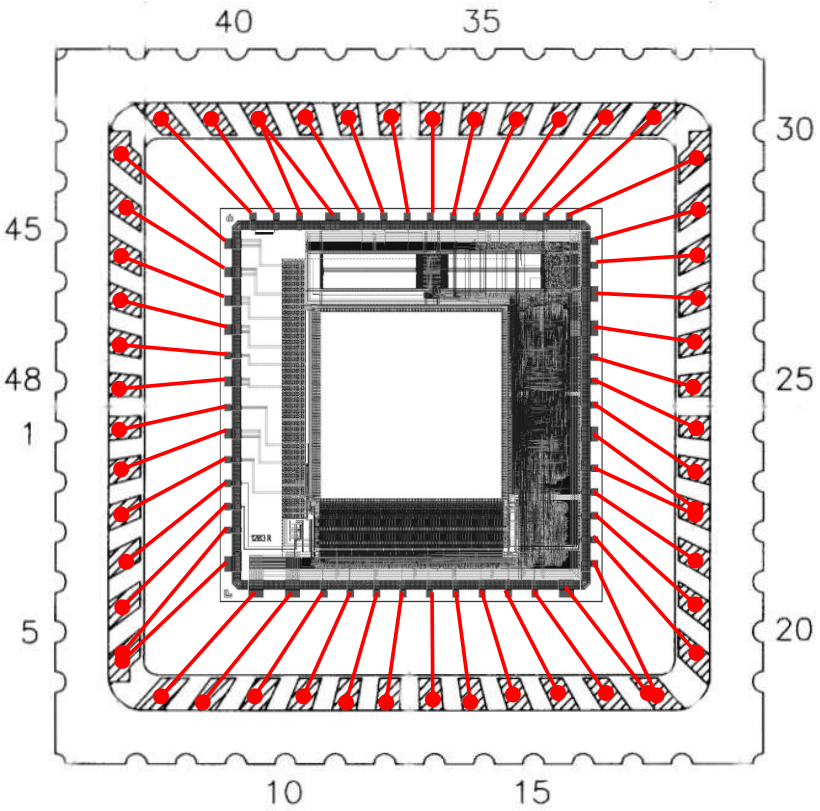
Test board connection circuit.



Package dimension (**JLCC-48**)


□ 10.00±0.15
□ 8.50±0.10
□ 7.50±0.10
4X 0.35 MIN. (0.50)
40
35
30
25
20
15
10
45
48
1
5
4X 0.75±0.15
4X R 0.50
4X R 0.20
1.00±0.10
0.40±0.05
0.40±0.05
0.20±0.05
LAYER-1
MP-2
MP-3
MP-4
4X P. 0.70X11=7.70±0.10
P. 0.70±0.10
8X 1.15 +0.25 -0.13
47X 0.80±0.18
48X 0.40±0.05
48X (R 0.15)
4X (R 0.15)
1.20±0.25
48X (0.60) (METALLIZED)
0.05
0.04
0.07
NOTES:
1. PLATING (ELECTROLYTIC):
Ni : 1.27~8.89 MICRON.
Au : 0.50 MICRON NOM.
2. BAKING TEST :
350 +10/-0°C FOR 180 +30/-0 SECONDS
IN OVEN.
3. WIRE BOND PAD CONNECTED TO CORRESPONDED OUTER PAD.
4. MISALIGNMENT OF METALLIZATION PATTERN IN CAVITY SHALL BE
ACCEPTED DUE TO LAYER MISALIGNMENT.

Bonding Diagram to JLCC-48.



Pin description

JLCC-48 pin #	Name	Function
1	VW	Output of internal DAC (VW)
2	VCC	Power for analog circuits, (3.3V)
3	VTX	Output of internal DAC (VTX)
4	RbotB	Test output
5	Rbot	Reference ADC input Low (0V)
6	DVSS	GND for I/O circuits, (0V)
7	VSS	GND for logical circuits, (0V)
8	VDD	Power for logical circuits, (1.8V)
9	nRST	Initializing Reset (Active low)
10	XI	Main Input Clock
11	SEU	Single Event Upset
12	eRUN	External RUN
13	SCS	SPI Chip Select
14	SCLK	SPI Clock
15	MOSI	SPI Master Output Slave Input
16	MISO	SPI Master Input Slave Output
17	BE	Broadcast Enable
18	DVDD	Power for I/O circuits, (3.3V)
19	Rup, (1.8V)	Reference ADC input High (1.8V)

20	RupB	Test output
21	VE	Test input signal, (0.5 … 1.8V)
22	DVSS	GND for I/O circuits, (0V)
23	DSYN	Image data synchronizing pulse
24	VSYN	Vertical synchronizing pulse
25	HSYN	Horizontal synchronizing pulse
26	VSS	GND for logical circuits, (0V)
27	VDD	Power for logical circuits, (1.8V)
28	Q2	Image data output [2]
29	Q0	Image data output [0] (LSB)
30	Q1	Image data output [1]
31	Q3	Image data output [3]
32	Q4	Image data output [4]
33	CRDY	Coordinate Ready output
34	Q5	Image data output [5]
35	LED	External light source synchronizing pulse
36	Q6	Image data output [6]
37	Q7	Image data output [7]
38	Q8	Image data output [8]
39	Q9	Image data output [9] (MSB)
40	DVDD	Power for I/O circuits, (3.3V)
41	TD2	Thermo Resistor output 2
42	TD1	Thermo Resistor output 1
43	VDR	Power for pixel array, (1.7V)
44	VDPIX	Power for CDS circuits, (1.8V)
45	VDA	Power for ADC/DAC analog circuits, (1.8V)
46	VDDA	Power for ADC logical circuits, (1.8V)
47	VRST	Output of internal DAC (VRST)
48	GND	GND for analog circuits, (0V)

Assembly image.