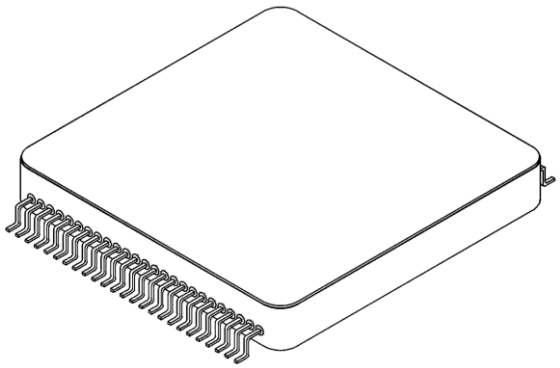
RAD HARD LOW VOLTAGE 10A SWITCHING REGULATOR WITH CURRENT SHARE

FEATURES

- Integrated Inductor
- Adjustable 0.6V to 4.0V Output, Greater than 10A
- 2 Phase Current Sharing Mode Enables Output Current in Excess of 20A
- Adjustable Frequency and Synchronization for Sensitive Applications
- Soft-Start, Logic Level Enable, PGOOD Flag, and Power On Reset Features Simplify Sequencing
- Simple Heat Sinking; Low Thermal Resistance, Pin Connected Case
- TID Hardened to 100 Krads
- Comparable to MSK5061RH



DESCRIPTION

A radiation-hardened adjustable output switching voltage regulator, the JTR5061. This regulator is an exceptionally easy to use device for many space power applications due to its wide input and output range, output current in excess of 10A, and complete features. The robust integrated inductor and passives components reduce design time and board size substantially. All internal components have been engineered to meet even the most rigorous dependability standards, reducing the risk of program design-in. The JTR5061 is housed in a 50-pin flatpack that is hermetically sealed. The JTR5061 series is housed in a 10 pin ceramic flatpack with a built-in aluminum base that saves space.

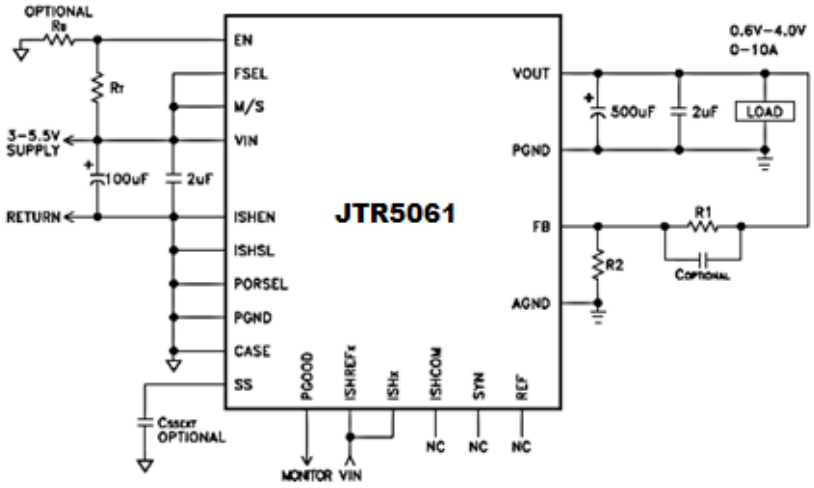
TYPICAL APPLICATIONS

- Low Voltage High Current Point of Load Regulation
- High Efficiency Satellite and space craft power supply
- High power FPGA, ASIC, µP, & Analog POL

Table 1. Pin description.

PIN	NAME	PIN	NAME
1	VIN1	26	PGND1/CASE
2	VIN2	27	PGND2
3	VIN3	28	PGND3
4	VIN4	29	PGND4
5	VIN5	30	PGND5
6	ISHA	31	VOUT1
7	ISHREFA	32	VOUT2
8	ISHB	33	VOUT3
9	ISHREFB	34	VOUT4
10	ISHC	35	VOUT5
11	ISHREFC	36	VOUT6
12	SS	37	VOUT7
13	PGOOD	38	VOUT8
14	ISHCOM	39	VOUT9
15	ISHSL	40	VOUT10
16	ISHEN	41	VOUT11
17	PORSEL	42	PGND6
18	SYNC	43	PGND7
19	M/S	44	PGND8
20	FSEL	45	PGND9
21	VIN6	46	PGND10
22	VIN7	47	AGND
23	VIN8	48	EN
24	VIN9	49	REF
25	VIN10	50	FB

TYPICAL APPLICATION CIRCUIT



ELECTRICAL SPECIFICATIONS

Table 2. Electrical specifications

Parameter	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
V_{IN} Threshold	V_{IN}		3.3	5	5.5	V
V_{IN} Hysteresis	$V_{IN(hys)}$		-	0.25	-	V
Feedback Voltage	V_{FB}	1A ≤ I_{OUT} ≤ 4.5A, V_{IN}=5V	0.59	0.60	0.61	V
Switching frequency	fsw	I_{OUT}=3A, V_{OUT}=3.3V	0.85	1.0	1.2	MHz
Soft Start Time	T_{SS}		-	2.3	-	ms
Efficiency	Eff	I_{OUT} = 5A, V_{OUT} = 3.3V, V_{IN}=5V	-	90	-	%
EN Pin Logic High Threshold Voltage	V_{ENH}	Disable	0.6	-	-	V
	V_{ENL}	Enable	-	-	1.2	
EN Pin Pull-Up Current	I_{EN}	V_{IN} =4V	-	65	185	uA
		V_{IN} =5V	-	73	211	
Current Limit	I_{LIM}	V_{IN}=V_{OUT}+1V	10	-	-	A
Thermal Shutdown Threshold	T_{SD}		125	130	-	°C
Quiescent Current	I_Q	I_{OUT} = 5A	-	50	70	mA
		Full Load	-	170	210	

APPLICATION NOTES

PIN FUNCTIONS

VIN – All of the internal circuitry's input supply pins are located on the VIN pins. These pins are subjected to high di/dt switching currents. Decouple VIN from PGND using a combination of high frequency ceramic capacitors and tantalum with a low ESR. To guarantee a low impedance buss and to reduce input voltage ripple, provide enough bulk capacitance.

PGND – The internal power ground plane is connected to the PGND pins. These pins are used to conduct high di/dt switching currents. Between the JTR5061 PGND, the input supply return, and the load, provide a constant low impedance ground link. Layouts that cause load return current to cross the AGND reference route should be avoided.

VOUT – The internal output inductor is linked to the VOUT pins. To reduce bus impedance, connect VOUT as near to the load as feasible. Connecting a low ESR bulk capacitance of 500 to 1000F to VOUT is usually enough to assure stable operation. To roll off high frequency gain, decrease switching noise, and slow load transients, some ceramic capacitance near the load is usually necessary. A combination of high frequency ceramic capacitors and tantalum with a low ESR is recommended. See the paragraph on Output Capacitor Selection.

AGND – For the internal control circuitry, the AGND pin offers a low noise signal reference. Connect AGND and PGND at the ground side of the load for optimal regulation performance.

PGND1/CASE – The JTR5061 casing and PGND are electrically linked to this pin.

FB – The FB pin is the error amplifier's inverting input. The 0.6V reference voltage and the voltage at this pin are utilized to servo to the current control loop set point. To program the output voltage, connect the FB pin to the center node and place a resistor divider between VOUT and AGND near the load. See the paragraph on Output Voltage Selection.

REF – The internal 0.6V reference voltage utilized in various circuit operations is represented via the REF pin. For current sharing applications, the reference voltage is pinched out. Connect the REF pins of the master and slave JTR5061s with a 10 resistor when using the 2 phase current sharing feature. This pin cannot be loaded in any other way.

FSEL – The JTR5061's switching frequency is programmed via the FSEL pin. For 1MHz operation, connect to VIN; for 500KHz operation, connect to PGND.

PORSEL – The JTR5061's power on reset thresholds are programmed via the PORSEL pin. For a 5V nominal input bus, connect to VIN; for a 3.3V nominal input bus, connect to PGND. Connect to PGND to create an input bus that ranges from 3 to 5.5 volts.

SS – The Soft Start pin allows for the management of turn-on surge currents as well as coincident and ratiometric tracking. The internal SS capacitor is charged by a 23A current source, which sets the output ramp rate to around 2.6mS. Reduce the output ramp rate by adding more capacitance. The slave ramp rate should be at least twice that of the master in two-phase current sharing applications. In the Start Up Considerations section, you'll find further application advice.

EN – The EN pin controls the regulator's on/off hysteresis. The regulator is enabled when this pin is driven over 0.6V. With an 11A current sink that is active until the pin voltage exceeds VREF, programmable hysteresis may be achieved. When controlling from a high-impedance source, use a capacitor to connect to ground. For further information, see the applications section.

PGOOD – When the regulator's output voltage falls outside of an 11 percent typical window, the PGOOD pin is pushed low. This status flag can be used to control supply and detect faults.

M/S – The purpose of the bidirectional SYNC pin is determined by the M/S input pin. For Master mode, connect M/S to VIN, where the SYNC pin is the master oscillator output. For Slave mode, connect M/S to PGND, and SYNC becomes an input.

SYNC – This pin drives the SYNC pin input of another JTR5061 with a square wave that is phase shifted 180° from the Master clock controlling the Master PWM circuits when SYNC is set as an output, M/S = VIN. When configured as an input, M/S = PGND, this pin clocks the PWM circuitry using the SYNC output from another JTR5061 or an external clock. If you're using an external clock, make sure it's SEE hardened and that the frequency is between 400kHz and 1.2MHz.

OUTPUT CAPACITOR

The output voltage ripple of the JTR5061 series voltage regulators can be reduced by connecting the output to ground with a filter capacitor. The best value for this capacitor varies depending on the application, however a minimum of 10F is

advised for best results. Placing a capacitor directly across the load can help increase transient load responsiveness.

ISHEN – The present sharing feature is enabled by the ISHEN pin. To use the existing sharing functions, connect to VIN. To disable the present sharing functionality, connect to PGND.

ISHSL – The ISHSL pin determines whether the JTR5061 is a current share master or slave. Connect to PGND to set the device as a master or if the device's existing sharing features aren't working. To set up the JTR5061 as a current share slave device, connect to VIN.

ISHCOM – A bidirectional communication connection between a current share Master and a current share Slave is known as ISHCOM. Tie the Master's ISHCOM to the Slave's ISHCOM if you're utilizing the current share. By resistively (8.5k) pushing ISHCOM up, the Master enables the Slave. By pushing ISHCOM low, the Slave informs the Master of an over-current fault condition. Connect a 47pF ceramic capacitor from ISHCOM to the PWB ground plane to reduce SET. This pin should be floating or connected to the PCB ground plane if current sharing is not being used. If ISHEN is low, ISHCOM is tri-stated.

ISHREFA, B, C – The ISHREFA/ISHREFB/ISHREFC pins supply a reference output current of 100A each when configured as a current share Master. The ISHREFA/ISHREFB/ISHREFC pins take a reference input current when configured as a current share Slave. This input current is used with the ISHA/ISHB/ISHC current to determine the Master's redundant A/B/C error amp output current for a current share Slave.If you're utilizing current sharing, link the MASTER's ISHREFA/ISHREFB/ISHREFC to the Slave's ISHREFA/ISHREFB/ISHREFC. Tie ISHREFA/ISHREFB/ISHREFC to VIN if you're not utilizing the current share. The purpose of the reference current is to decrease the influence of external noise coupling on ISHA/ISHB/ISHC. Prior to a valid POR and when ISHEN = PGND, ISHREFA/ISHREFB/ISHREFC are tri-stated.

ISHA, B, C – The ISHA/ISHB/ISHC pins are outputs that give a current equivalent to 25 times the redundant A/B/C error amp output currents plus ISHREFA/ISHREFB/ISHREFC (nominally 100A each) when set as a current share Master. The ISHA/ISHB/ISHC pins are inputs that become the Slave's redundant A/B/C error amp output current when configured as a current share Slave. If you're utilizing a current share, link the Master's ISHA/ISHB/ISHC to the Slave's ISHA/ISHB/ISHC. Tie ISHA/ISHB/ISHC to DVDD if you're not utilizing the present share. Prior to a valid POR and when ISHEN = PGND, ISHA/ISHB/ISHC are tri-stated.

POWER SUPPLY BYPASSING

The input bus current is pulled in approximately trapezoidal pulses with very rapid edge speeds, resulting in a large frequency spectrum. To give a low impedance to the high frequency components of the wave form and trap them local to the regulator, high quality low ESR/ESL ceramic capacitors connected directly across the VIN and PGND pins are recommended. Radiated EMI can be reduced by reducing the size of the VIN-CIN-PGND loop. With a high internal ceramic capacitance, the JTR5061 simplifies application. The AC component of the switching current is fed into the regulator through internal and external input capacitors. The RMS ripple current detected by the input capacitors is rather large, reaching a maximum of 0.5 times Iout at about 50% duty cycle. To decrease ripple voltage perceived by the device and guarantee steady operation, sufficient bulk capacitance must be supplied. VIN ripple should be less than 3 to 5% of VIN as a general rule of thumb. To provide adequate voltage and ripple current derating, the bulk input capacitors will most likely be selected using a parallel mix of multiple tantalum and ceramics. If those conditions are met, there will usually always be enough bulk to reduce ripple voltage and assure stable operation.

OUTPUT CAPACITOR SELECTION

At 1MHz, a total of 500uF of low ESR capacitance placed near the JTR5061 has been demonstrated to offer adequate stability margins. However, due to physical and practical constraints, at least some bypass capacitance near the load may be required. A transient voltage signal proportional to the amount of the load step will arise due to the capacitor parasitic ESR and ESL, non-zero impedance between the regulator output and the load terminals, and finite bandwidth. Transient voltage excursions can be mitigated by adding low ESR output capacitance. Capacitor selection should be done with caution so that the loop maintains a sufficient stability

margin. If running at switch frequencies below 750kHz, more output capacitance will be necessary to reduce loop bandwidth and enhance stability margins. In this case, a temperature adjustment of 220 to 330 degrees Fahrenheit is usually sufficient. For further details, look at the normal performance curves.

OUTPUT VOLTAGES SELECTION

The following equation governs the output voltage:

$$V_{OUT}=V_{REF} \times \left[1 + \frac{R1}{R2}\right]$$

Solving for R1:

$$R1 = R2 \times \left[\frac{V_{OUT}}{V_{REF}} - 1\right]$$

Power and leakage current effects are generally minimized by using resistors in the 1K to 5K range. R–C networks can be used in tandem with R1 and/or R2 to provide some loop compensation. Analysis and measurement should be used to verify any compensatory attempts.

START UP CONSIDERATION; POR, EN, SS AND PGOOD

Any buck switching regulator's input has a negative input resistance, which means that as the input voltage drops, the input current rises. In addition, the current required to charge the output capacitors is proportional to the total output capaci-tance and the rate at which the output voltage may grow. In intermediate power systems that aren't intended to manage these extra currents, a lockout scenario might develop upon startup. The fact that many FPGAs, ASICs, and processors impose stringent limitations on the rise time and sequence of supply rail voltages further complicates matters. The JTR5061 includes numerous features that are especially intended to make these difficulties easier to manage. The JTR5061's Power On Reset feature stops the soft start cycle from starting until VIN has climbed beyond the PORSEL pin strap's threshold. For help choosing the right POR threshold for your application, consult the Electrical Specifications Table and the pin functional description.

When driven above VREF, the EN pin activates the regulator output, making it easy to perform supply sequencing. The user programmable EN pin Hysteresis provides noise immunity. Through a resistor divider, connect the control signal to EN. The top bound of the hysteresis loop is created when an 11A current source is active until the EN pin voltage passes 0.6V. Once EN surpasses 0.6V, the current source is disabled, creating the hysteresis loop's bottom bound. Define the EN pin thresholds and hysteresis using the formulae below.

$$V_{ENABLE}=\left(V_{REF} \times \left[1+ \frac{R_T}{R_B}\right]\right) + \left[I_{EN} \times R_T\right]$$

$$V_{DISABLE}= V_{REF} \times \left[1 + \frac{R_T}{R_B}\right]$$

$$EN_{HYST}= V_{ENABLE} - V_{DISABLE}$$

A soft start cycle will be started after the POR and EN requirements have been met. By regulating the output voltage ramp rate, the Soft Start circuit minimizes the surge current needed to charge the output capacitors.

This functionality may also be used to construct coincident and ratiometric tracking supplies, which are required by many modern digital systems. During startup, the error amplifier reference voltage is clamped to the SS pin, and the SS pin capacitor is charged using a 23A current source. The soft start ramp rate can be varied between 2.6 and 214 milliseconds. Determine the desired ramp rate and apply the following equation to find the soft start capacitor that corresponds.

$$C_{SSEXT}= \frac{T_{SS} \times I_{SS}}{V_{REF}} - 0.1uF$$

The soft start ramp rate can be varied between 2.6 and 214 milliseconds. Determine the desired ramp rate and apply the following equation to find the soft start capacitor that corresponds.

SYNCHRONIZATION

External clocks in the range of 400kHz to 1.2MHz can be used to synchronize the JTR5061. Precision system designers may now direct switching noise away from sensitive bands, minimize supply ripple current, and remove power supply beat frequencies caused by numerous free running switching regulators.

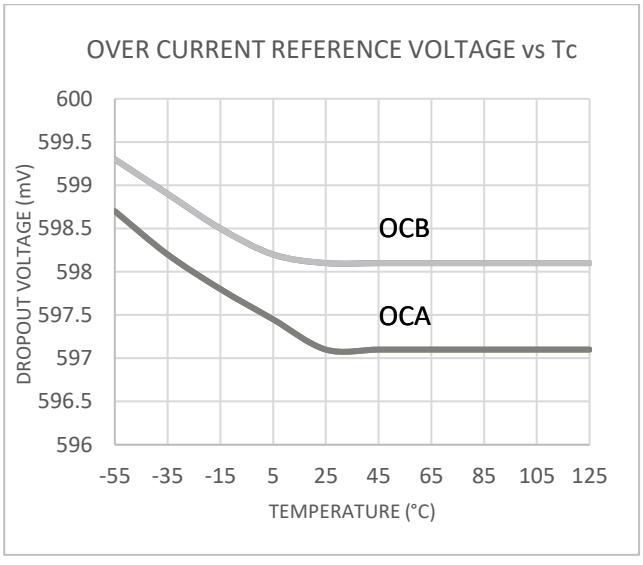
To synchronize the JTR5061 with another JTR5061, connect the master and slave devices' M/S pins to VIN and PGND, respectively, and the SYNC pins directly. A RAD HARD clock

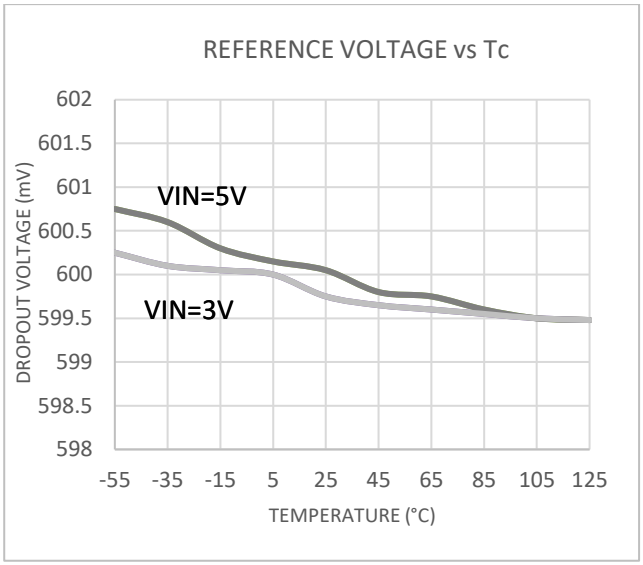
generator can also be used to synchronize one or more JTR5061.

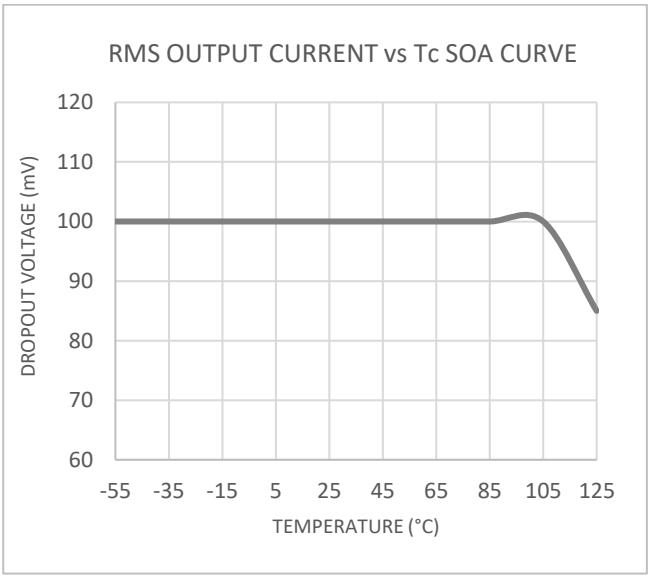
CURRENT SHARING

Two JTR5061 can be used together to create a reliable fault-tolerant two-phase supply with a current capacity of over 20A. A redundant Current Sharing bus balances the load current between the two devices and relays any fault conditions in this mode. One JTR5061 is labeled as the Master, while the other is marked as the Slave. The ISHSL pins for the Master and Slave are linked to PGND and VIN, respectively. VIN is linked to the ISHEN pins on both the Master and Slave. From the Master to the Slave, the SYNC, ISHA, ISHB, ISHC, ISHREFA, ISHREFB, ISHREFC, ISHCOM, and FB pins are linked, and the REF pins are bound with a 10 resistor. The load current capacity of the 2 phase current regulator roughly doubles when configured this way, with just the Current Share Match tolerance limiting the load current capacity. The JTR5061 run 180° out-of-phase in this Master/Slave arrangement to reduce input ripple current, essentially functioning as a single IC at double the switching frequency. Under idealized conditions, the output ripple voltage terms can also cancel out completely, resulting in a relatively quiet supply rail over a wide range of frequencies. The Master phase utilizes the falling edge of the SYNC clock to start the Master switching cycle with the non-overlap period before the rising edge of LX, whereas the Slave phase internally inverts the SYNC input and starts its switching cycle with the falling edge of the inverted copy. Whether the Master phase is configured for an external clock (Master M/S = PGND) or an internal clock (Master M/S = VIN), this is unaffected. The two phase regulator is controlled by the Master Error Amplifier and Compensation, while the Slave Error Amplifier is deactivated.

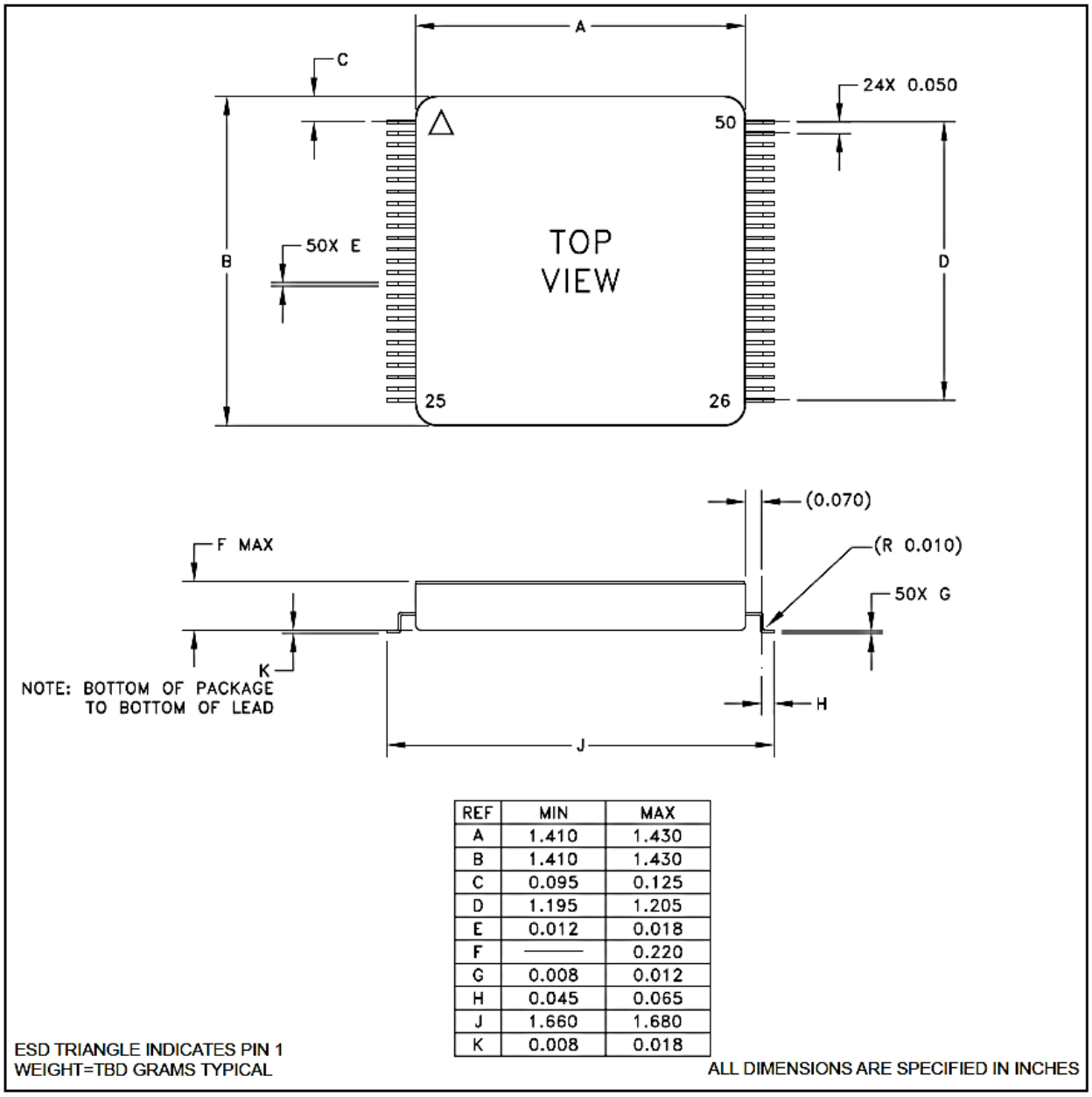
TYPICAL PERFORMANCE CURVES







MECHANICAL SPECIFICATION



REF	MIN	MAX
A	1.410	1.430
B	1.410	1.430
C	0.095	0.125
D	1.195	1.205
E	0.012	0.018
F	———	0.220
G	0.008	0.012
H	0.045	0.065
J	1.660	1.680
K	0.008	0.018

ESD TRIANGLE INDICATES PIN 1
WEIGHT=TBD GRAMS TYPICAL

ALL DIMENSIONS ARE SPECIFIED IN INCHES