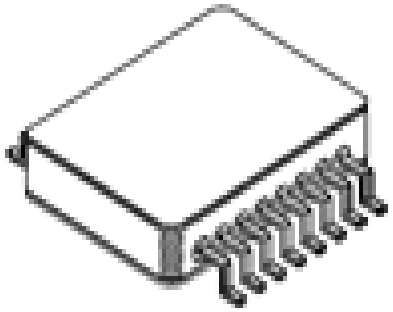
RAD HARD 4.5A, 500KHz STEP DOWN SWITCHING REGULATOR CONTROLLER

FEATURES

- 500KHz Constant Switching Frequency
- Synchronizable to 1MHz
- 4.5A Integrated Switch
- Input Voltage Range from 4.5V to 16V
- Cycle by Cycle Current Limit
- Output Voltages Down to 1.21V
- TID Hardened to 100 Krads
- Comparable to MSK5059RH



DESCRIPTION

The JTR5059 is an easy-to-use 500KHz Radiation-hardened step-down switching regulator controller that is capable of driving up to 4.5 A of load current from a supply voltage ranging from 4.5 V to 16 V. A fixed switching frequency of 500 kHz allows for the use of smaller inductors, reducing the footprint of board space required for a particular design. With the 4.5A integrated switch, the designer is left with only a few application-specific components to choose from. The JTR5059 makes it easier to create high-efficiency radiation-hardened switching regulators with minimal board footprint. The device comes with either straight or gull wing leads and is packaged in a hermetically sealed 16 pin flatpack.

Table 1. Pin description.

PIN	NAME	PIN	NAME
1	VINA	9	VC
2	VINB	10	SHDN
3	VINC	11	SYNC
4	VIND	12	SWE
5	VINE	13	SWD
6	BOOST	14	SWC
7	FB	15	SWB
8	GND	16	SWA

TYPICAL APPLICATIONS

- POL Applications
- Satellite System Power Supply
- Step Down Switching Regulator
- Microprocessor, FPGA Power Source
- High Efficiency Low Voltage Subsystem Power Supply

TYPICAL APPLICATION CIRCUIT

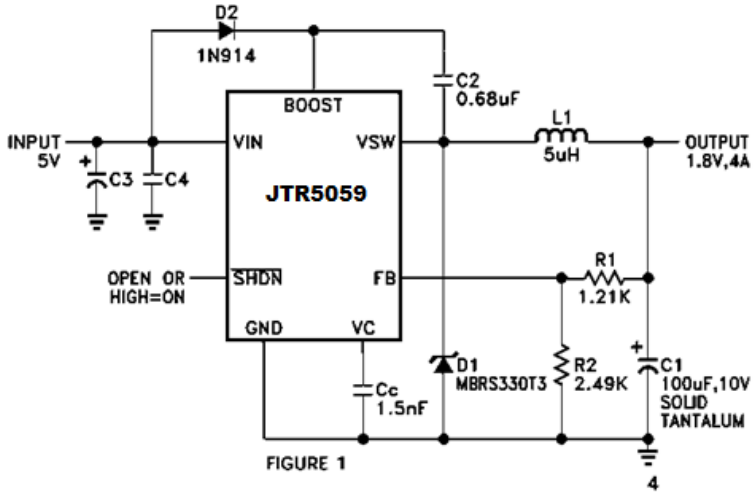


FIGURE 1

ELECTRICAL SPECIFICATIONS

Table 2. Electrical specifications

Parameter	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
V_{IN} Threshold	V_{IN}		4.5	5	16	V
V_{IN} Hysteresis	$V_{IN(hys)}$		-	0.5	-	V
Feedback Voltage	V_{FB}	1A ≤ I_{OUT} ≤ 4.5A, V_{IN}=5V	1.19	1.21	1.23	V
Switching frequency	fsw	I_{OUT}=3A, V_{OUT}=3.3V	0.45	0.5	1.0	MHz
Soft Start Time	T_{SS}		-	0.9	-	ms
Efficiency	Eff	I_{OUT} = 2.5A, V_{OUT} = 3.3V, V_{IN}=5V	-	85	-	%
SHDN Pin Logic High Threshold Voltage	V_{ENH}	Disable	-	-	0.6	V
	V_{ENL}	Enable	1.2	-	-	
SHDN Pin Pull-Up Current	I_{EN}	V_{IN} =5V	-	70	200	uA
		V_{IN} =10V	-	90	300	
Current Limit	I_{LIM}	V_{IN}=V_{OUT}+1V	4.5	-	-	A
Thermal Shutdown Threshold	T_{SD}		125	130	-	°C
Quiescent Current	I_Q	I_{OUT} = 1A	-	40	50	mA
		Full Load	-	100	150	

APPLICATION NOTES

PIN FUNCTIONS

VIN - The VIN pins supply power to the internal control circuitry and regulator by connecting to the collector of the internal power switch. During switch on and off transitions, these pins have a very high di/dt. To reduce voltage spikes, high frequency decoupling capacitors are advised. For optimal performance, all five VIN pins should be linked to a low impedence source.

SW - The SW pins are linked to the internal power transistor's emitter. When the power switch is turned on, these pins rise to the input voltage and are driven negative when the switch is turned off. The catch diode clamps the negative voltage, ensuring that it does not go below -0.8V. For optimal performance, all five SW pins must be connected.

BOOST - The BOOST pin delivers a higher driving voltage to the power transistor's base than VIN. Using a voltage larger than VIN guarantees that the power switch is hard-saturated, which improves overall efficiency. To store charge, connect a capacitor between BOOST and SW. To charge the capacitor during the power switch's off period, connect a diode between VIN and BOOST.

FB - The major function of the FB (feedback) pin is to set the output voltage. When the output voltage is at the desired level, use a resistive divider from VOUT to GND to set the voltage at the feedback pin to 1.21V. Two more functionalities are provided by the FB pin. The switch current limit is decreased if the voltage at the FB pin falls below 0.8V. When the voltage at the FB pin falls below 0.7V, the switching function is activated. The switching frequency is decreased and sync is deactivated when the voltage at the FB pin falls below 0.7V. At VFB=0.4V, the switching frequency drops to around 100KHz.

GND - The GND pin functions as a reference to the error amplifier and serves as a return channel for all internal control current. To achieve effective regulation, it must be at the same voltage potential as the load return. To reduce voltage drops and regulation error, keep current on the ground between the load and the JTR5059 to a minimum and utilize thick copper traces.

VC - The VC pin is the peak current comparator's input and the error amplifier's output. This pin is generally used for frequency correction, but it may also be used to cap current or override the inbuilt error amplifier control. When under moderate load, the pin voltage is generally about 1V, and when under heavy load, it is approximately 2V. The regulator will be turned off if the pin is driven low. The output current will be increased if the voltage is raised. When pushing the VC pin high, the current entering it must be restricted to 4mA.

SHDN - There are two shutdown functions for the SHDN (shutdown) pin. When the voltage on the pin falls below 2.38V, the first function stops switching (nominal). When the voltage falls below 0.4V, the second mode causes a complete shutdown, reducing power usage (nominal). For regular functioning, pull this pin high or leave it open. UVLO functions can leverage the 2.38V threshold by connecting VIN and GND to a resistive divider that keeps the pin voltage below 2.38V until VIN climbs to the lowest required voltage.

SYNC - To synchronize the oscillator with an external clock, utilize the SYNC pin. It may be operated at any frequency between the free run frequency (500KHz nominal) and 1MHz and is logic compatible. To achieve good synchronization, the duty cycle of the input signal must be between 10% and 90%. If the SYNC pin isn't in use, connect it to GND.

SETTING THE OUTPUT VOLTAGE

A simple resistor divider network is used to adjust the output voltage of the JTR5059: see Figure 1. (Typical Application Circuit). To split the required output down to equal VFB (1.21V nominal) at the FB pin, use the resistor settings. To reduce output error due to FB pin bias current below 0.1 percent, use a 2.5K or lower value resistor for R2.

VOUT=VFB*(1+R1/R2)

R1=R2*(VOUT/VFB-1)

SELECTING THE INDUCTOR

The inductor is used to reduce the square pulses at the SW pin to a linear ripple that is acceptable. At various input and output voltages, the inductance value will restrict the maximum possible current. In the typical performance curves portion of this data sheet, look for "Maximum Load Current." Make the initial value selection using the curves. Determine the peak inductor current by using the following formula:

IPK=IOUT+VOUT*(VIN-VOUT)/(2*f*L*VIN)

Where:

f=the switching frequency in Hz

L=inductor value in Henries

Select an inductor what will not saturate at worst case peak current. Calculate the peak to peak inductor current ripple as follows:

IP-P=VOUT*(VIN-VOUT)/(f*L*VIN)

Nearly all of the current ripple will be seen by the output capacitance. See selecting the output capacitor.

Overcurrent protection is provided by the JTR5059 series through the use of a timed latch off circuit. The internal latch timeout is triggered by an overcurrent condition. To allow for start up surge currents, the timeout is approximately 5.5mS at 25°C. If the overcurrent condition remains at the end of the timeout cycle, the regulator will latch off until the latch is reset. Reset the latch by pulling the shutdown pin high or cycling VIN off then back on. A thermal limit condition will trigger the latch with no time out delay.

SELECTING THE OUTPUT CAPACITOR

The output capacitor reduces the ripple current from the inductor to a level that the load can handle. The ESR of the output capacitor is the most important element in determining voltage ripple. The following is a rough estimate of the voltage ripple:

VP-P=IP-P*ESR

The typical ESR range for an JTR5059 application is between 0.05 and 0.20 ohm. Capacitors within these ESR ranges typically have enough capacitance value to make the capacitive tern of the ripple equation insignificant. The capacitive term of the output voltage ripple lags the ESR term by 90° and can be calculated as follows:

VP-P(CAP)=IP-P*(8*f*C)

Where:
C=output capacitance in Farads

Choose a capacitor (or a set of capacitors) that can withstand the worst-case ripple current while still allowing for enough de-rating. When employing numerous capacitors in parallel to accomplish ESR and/or total capacitance sharing, if all of the capacitors are the same kind and ideally from the same lot, the ripple current between them will be about similar.Low ESR tantalum capacitors are recommended over aluminum electrolytic. The zero created by the ESR of the capacitor is necessary for loop stabilty. A small amount of ceramic capacitance close to the load to decouple high frequency is acceptable but it should not cancel the ESR zero.

PROVIDING BOOST DRIVE

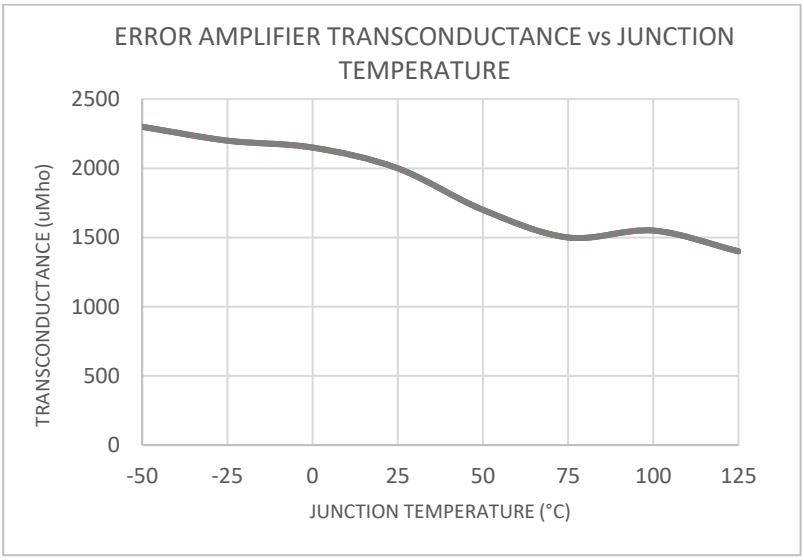
For the power transistor, the BOOST pin delivers drive larger than VIN. When the power switch is turned off, the boost capacitor is charged to the input voltage through a switching diode, as shown in Figure 1. The SW node rises to VIN when the power switch is turned on, and the boost capacitor delivers current to operate the power transistor. A 0.27F capacitor would usually suffice, however smaller capacitors can be used if necessary. The following equation provides a rough estimate of the absolute lowest value, but it should be used with caution because it does not account for all worst-case and secondary circumstances.

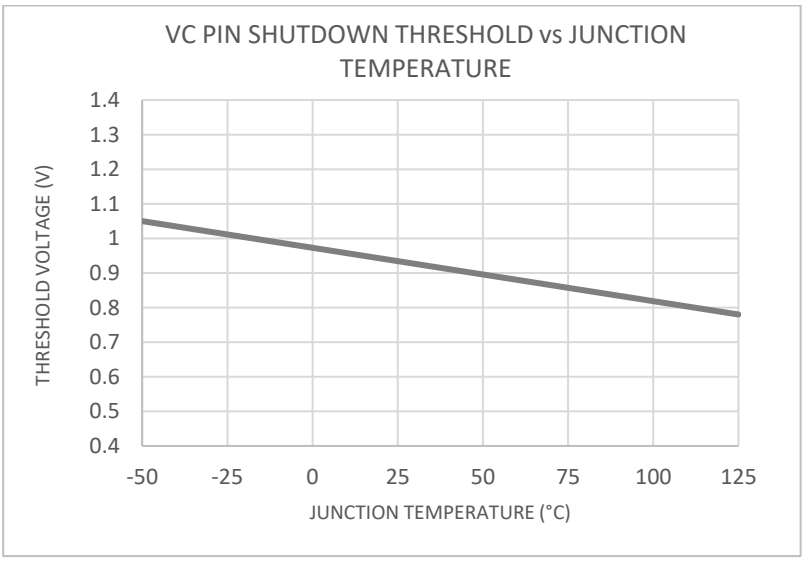
CMIN=(IOUT/50)*(VOUT/VIN)/f*(VOUT-2.8V)

COMPENSATING THE LOOP

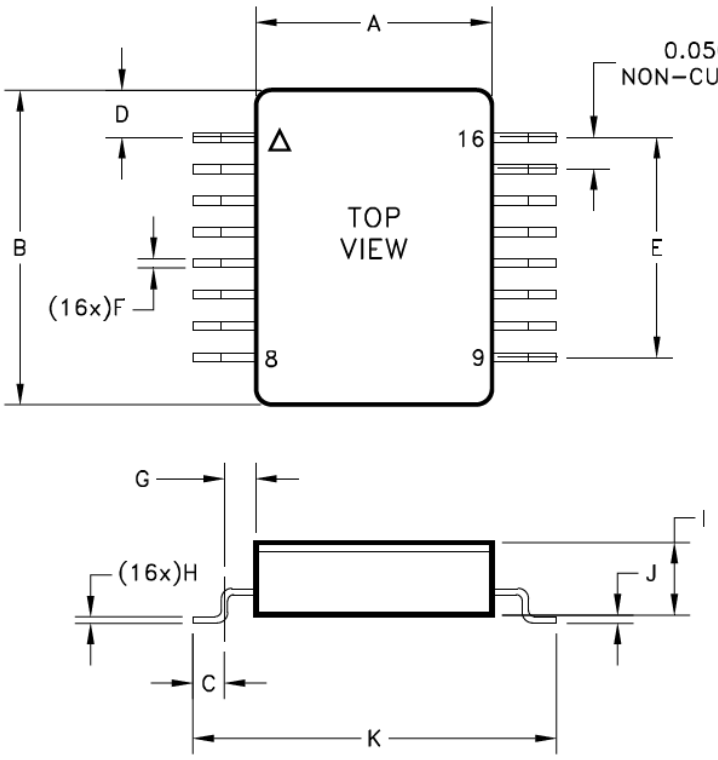
A transconductance of gm=5.3A/V may be used to represent the current mode power stage from the VC node to the SW node. The product of the transconductance and the load resistance determines the DC output gain. As the frequency rises, the output capacitance reduces the gain until the ESR reaches zero. The error amplifier may be represented as a 1000Mho transconductance with a 2K output impedance in parallel with a 12pF capacitor. To correct the loop, a simple 1000 to 2000pF capacitor is usually sufficient, but more complicated compensation methods are also possible.

TYPICAL PERFORMANCE CURVES





MECHANICAL SPECIFICATION



REF	MIN	MAX
A	0.365	0.385
B	0.490	0.510
C	0.045	0.055
D	0.075 REF	
E	0.345	0.355
F	0.012	0.018
G	0.050 REF	
H	0.008	0.012
I	———	0.115
J	0.008	0.018
K	0.550	0.600

NOTE: "J" IS MEASURED FROM BOTTOM OF PIN TO BOTTOM OF CASE.

ESD TRIANGLE INDICATES PIN 1
WEIGHT = TBD GRAMS TYPICAL